WHAT IS CLAIMED IS:

1. A semiconductor package comprising:

a first substrate having a die receiving area, a first adhesive layer, a window opening, and a plurality of conductive traces;

a first semiconductor die, having two sides, with an electrically active side being mounted to said substrate through the first adhesive layer within said die receiving area, to electrically couple said first semiconductor die to said conductive traces;

a second adhesive layer having a first side attached to an electrically inactive side of said first semiconductor die;

a second substrate having a die receiving area and a plurality of conductive traces and terminals;

a last adhesive layer having a first side attached to a side of said second substrate with said terminals;

a last semiconductor die, having two sides, with an electrically inactive side being mounted to the second side of said third adhesive layer, and an electrically active side being electrically coupled to said conductive traces of said first or second substrate directly or through a redistribution device;

an encapsulant to encapsulate said semiconductor dies and electrical coupling; and

signal transferring interconnects to transfer an electrical signal from said conductive traces to the exterior of the package.

2. The semiconductor package according to claim 1, wherein said first semiconductor die includes a plurality of bond pads, whereby said bond pads are positioned within the window opening of said first substrate.

3. The semiconductor package according to claim 1, wherein said first semiconductor die includes a plurality of bond pads, whereby said bond pads are not positioned within the window opening of said first substrate, said bond

pads being electrically relocated to the window opening by a redistribution device.

4. The semiconductor package according to claim 1, wherein said last semiconductor die has a plurality of bond pads, whereby said bond pads are positioned near the periphery of said last semiconductor die.

5. The semiconductor package according to claim 1, where said last semiconductor die has a plurality of bond pads, whereby said bond pads are not positioned near the periphery of said last semiconductor die, said bond pads being electrically relocated to the periphery of said last semiconductor die by a redistribution device.

6. The semiconductor package according to claim 5, wherein said redistribution device includes a wafer redistribution layer.

7. The semiconductor package according to claim 5, wherein said redistribution device includes a metallic interposer with a plurality of conductive traces, attached to the active surface of the last semiconductor die with an adhesive, with a plurality of electrical couplings from the bond pads to the metallic interposer.

8. The semiconductor package according to claim 5, wherein said redistribution device includes a metallic interposer with a plurality of conductive traces, attached to the active surface of said last semiconductor die with an adhesive, and a plurality of electrical couplings from the bond pads to the metallic interposer.

9. The semiconductor package according to claim 8, wherein said adhesive layer is an adhesive paste or coating.

10. The semiconductor package according to claim 8, wherein said adhesive layer is an adhesive film.

11. The semiconductor package according to claim 1, wherein the size of said first semiconductor die may be smaller, equal to, or greater than the size of said last semiconductor die.

12. The semiconductor package according to claim 1, wherein said electrical coupling from said first semiconductor die to said first substrate is by wire bond.

13. The semiconductor package according to claim 1, wherein said electrical coupling from said first semiconductor die to said first substrate is by a TAB method.

14. The semiconductor package according to claim 1, further comprising direct wire bonding from the bond pads of said last semiconductor die to the first or second substrate without going through any redistribution device.

15. The first semiconductor die is electrically coupled to the first substrate by a flip chip method.

16. The semiconductor package according to claim 1, wherein said last semiconductor die is electrically coupled to said second substrate by a flip chip method.

17. The semiconductor package according to claim 1, wherein said last semiconductor die is stacked with an inactive side facing an inactive side of a flip chip semiconductor die on said second substrate.

18. The semiconductor package according to claim 1, wherein said second substrate is formed of any of the following materials including silicon, ceramic, laminate, aluminum, and any material that can be manufactured with a plurality of conductor traces.

19. The semiconductor package according to claim 1, wherein said second substrate is formed of a thin laminate, a flexible circuit, or a lead-frame and processed to increase rigidity for attachment and an electrical interconnection process.

20. The semiconductor package according to claim 1, wherein said second substrate has terminals along its periphery allowing interconnects to convey electrical signals to and from said last semiconductor die and said first substrate at any side of said last semiconductor die.

21. The semiconductor package according to claim 1, wherein said second substrate includes a plurality of conductive traces having the terminals positioned in optimum positions along its periphery such that when wire bonding from the terminal positions to said first substrate allow the shortest paths to the package external pins.

22. The semiconductor package according to claim 1, wherein said second substrate includes a plurality of conductive traces having the terminals positioned in optimum positions along its periphery such that wire bonding from the terminals positions to said first substrate allow shortest paths to the interconnection from said first semiconductor die.

23. The semiconductor package according to claim 1, wherein a plurality of dies are positioned between said first and last semiconductor die, whereby a semiconductor die between said first and said last semiconductor die are electrically coupled to said first or second substrate.

24. The semiconductor package according to claim 23, wherein the size of said plurality of dies can be smaller, equal to, or greater than the size of said first or last semiconductor die.

25. The semiconductor package according to claim 1, further comprising a spacer in the stacking of the semiconductor dies.

26. The semiconductor package according to claim 1, wherein said window opening comprises a plurality of openings in said first substrate coinciding with the bond pads of said first semiconductor die.

27. The semiconductor package according to claim 1, wherein said encapsulant is a liquid encapsulant.

28. The semiconductor package according to claim 1, wherein said encapsulant is a transfer molded molding compound.

29. The semiconductor package according to claim 1, wherein said encapsulant is applied to the package to cure.

30. The semiconductor package according to claim 1, wherein said encapsulant comprises a lid to cover said semiconductor die and electrical coupling.

31. The semiconductor package according to claim 1, wherein all the adhesive layers can be pre-attached to a receiving area or to the respective matching side of the part to attach to the receiving area.